# System Architect – Performance Benchmarking & Data Infrastructure

Beaverton, Oregon (hybrid) | Exceptional remote applicants will be considered

Level: Senior/Staff

## About the Role

Silicon45 is developing a distributed heterogeneous acceleration platform that combines CPUs, GPUs, DPUs, and FPGAs to improve the performance and efficiency of data-intensive workloads. We are seeking a System Architect to lead end-to-end performance characterization, benchmarking, and hardware-software co-design for our Si45 System Accelerator product.

## What You Will Do

- **Characterize the complete data path.** Trace and measure data movement from NIC and storage ingress through Linux I/O, CPU caches and DRAM, NUMA domains, PCIe, accelerator memory, local NVMe, and SAN storage.
- **Find the real system bottleneck.** Use system telemetry and profiling to isolate CPU saturation, memory-bandwidth pressure, cache and NUMA penalties, PCIe congestion, storage queueing, network limits, lock contention, and serialization or data-copy overhead.
- **Own benchmark methodology.** Define repeatable single-node and multi-node baselines, A/B tests, representative datasets, warm/cold conditions, concurrency levels, and automated performance-regression suites.
- **Benchmark database workloads.** Develop and tune representative kdb+/q, PostgreSQL, SQL/analytical, and vector-search workloads; interpret query plans, access patterns, indexing, partitioning, and operator-level cost.
- **Evaluate acceleration placement.** Determine when workloads should be accelerated at network ingress, within the database/query path, through FPGA/GPU/DPU offload, or through a combination of streaming, caching, and compute acceleration.
- **Quantify end-to-end benefit.** Measure p50/p95/p99 latency, throughput, CPU utilization, memory bandwidth, PCIe traffic, storage IOPS/latency, network utilization, and power; distinguish kernel speedup from true application and batch-time improvement.
- **Guide hardware-software co-design.** Work with FPGA, software, networking, and database engineers to define data-flow interfaces, buffer strategies, partition sizes, concurrency, scheduling, and offload break-even points.

## Minimum Qualifications

- 5+ years in systems architecture, performance engineering, database infrastructure, distributed systems, or high-throughput data platforms.
- Expert understanding of x86 server architecture, CPU caches, DDR memory systems, NUMA, PCIe topology, interrupts, DMA, and Linux process/thread scheduling.
- Deep Linux performance and I/O knowledge across networking, block I/O, filesystems, NVMe, storage queues, memory management, and SAN-attached systems.
- Strong hands-on benchmarking and profiling skills, including experimental design, tracing, hardware performance counters, latency distributions, and root-cause analysis.
- Experience with database/query performance - such as kdb+/q, PostgreSQL, SQL engines, Spark, or other distributed analytical systems - and the ability to dissect execution plans and data-access behavior.
- Ability to reason quantitatively across hardware and software layers, performance models and benchmarked backed architecture recommendations, and translate into architecture and product decisions.

## Preferred Qualifications

- Hands-on CPU, GPU power, thermal and performance evaluation and accelerator-offload architecture.
- PCIe Gen4/Gen5, CXL concepts, IOMMU, pinned memory, peer-to-peer transfers, RDMA, kernel bypass, or high-speed Ethernet/InfiniBand data paths.
- kdb+/q performance engineering, time-series or market-data systems, columnar analytics, or vector databases.

## Compensation & Application

**Compensation:** Base salary plus equity, medical insurance, and 401(k).

**Apply:** Send your resume or CV to jobs@silicon45.com with a short description of one or two performance-critical systems you personally designed or optimized, including the bottleneck, your change, and the measurable result. Please do not include confidential information.

***Silicon45 is an equal opportunity employer.***